

Figure 1 - Redundant Clock Module Block Diagram



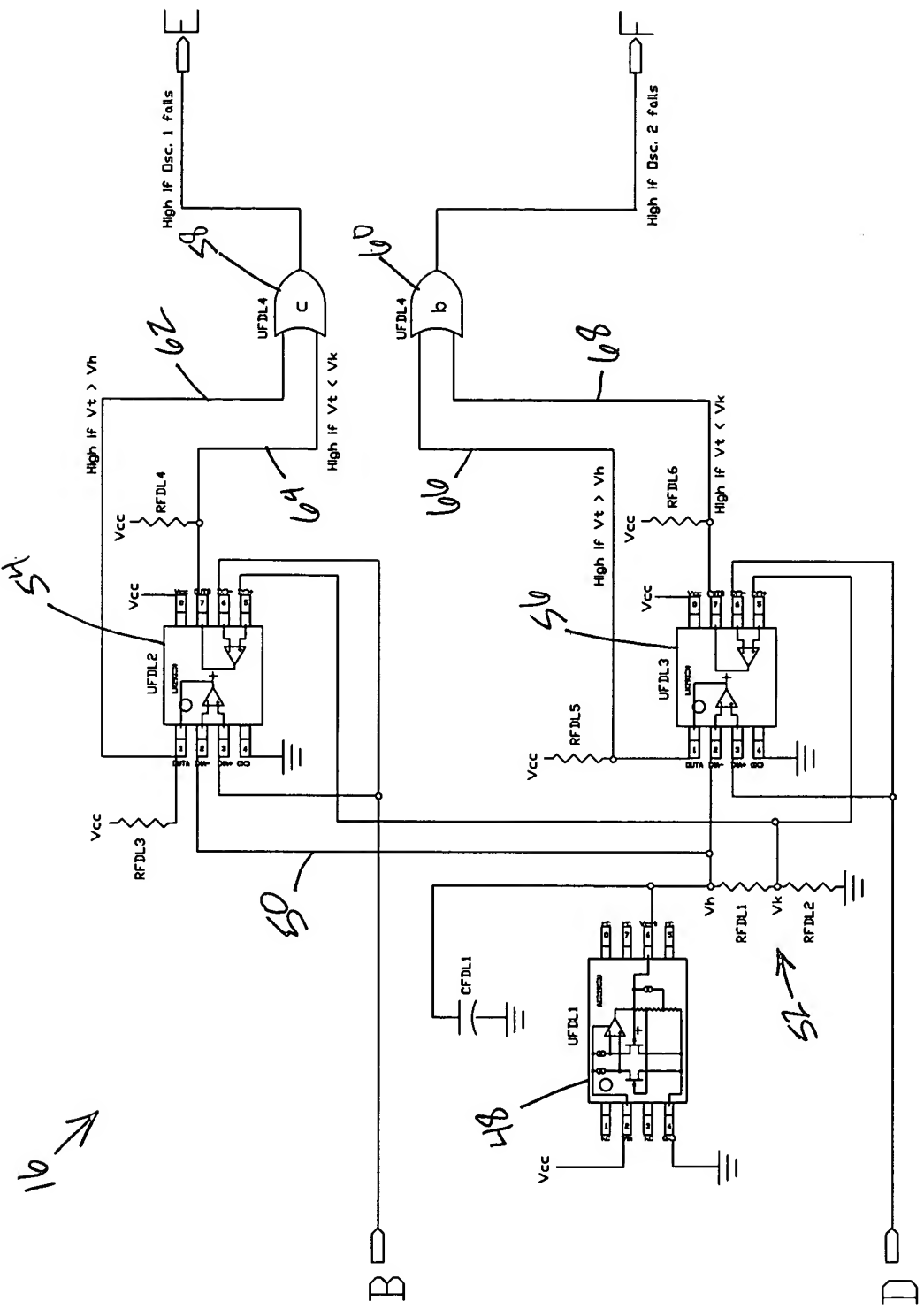


Figure 3 Frequency Detect Logic Stage



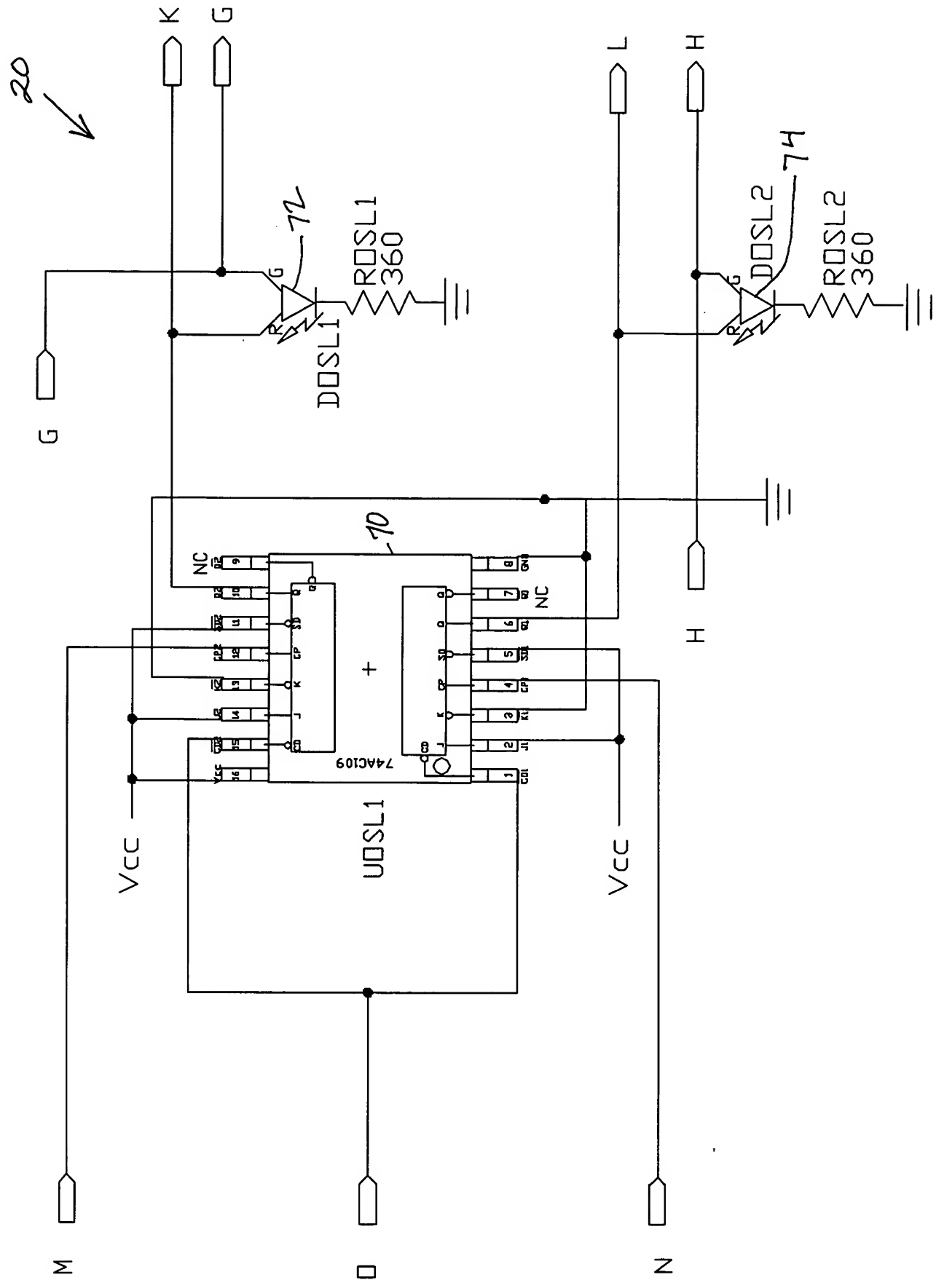


Figure 5 Oscillator Select Logic Stage

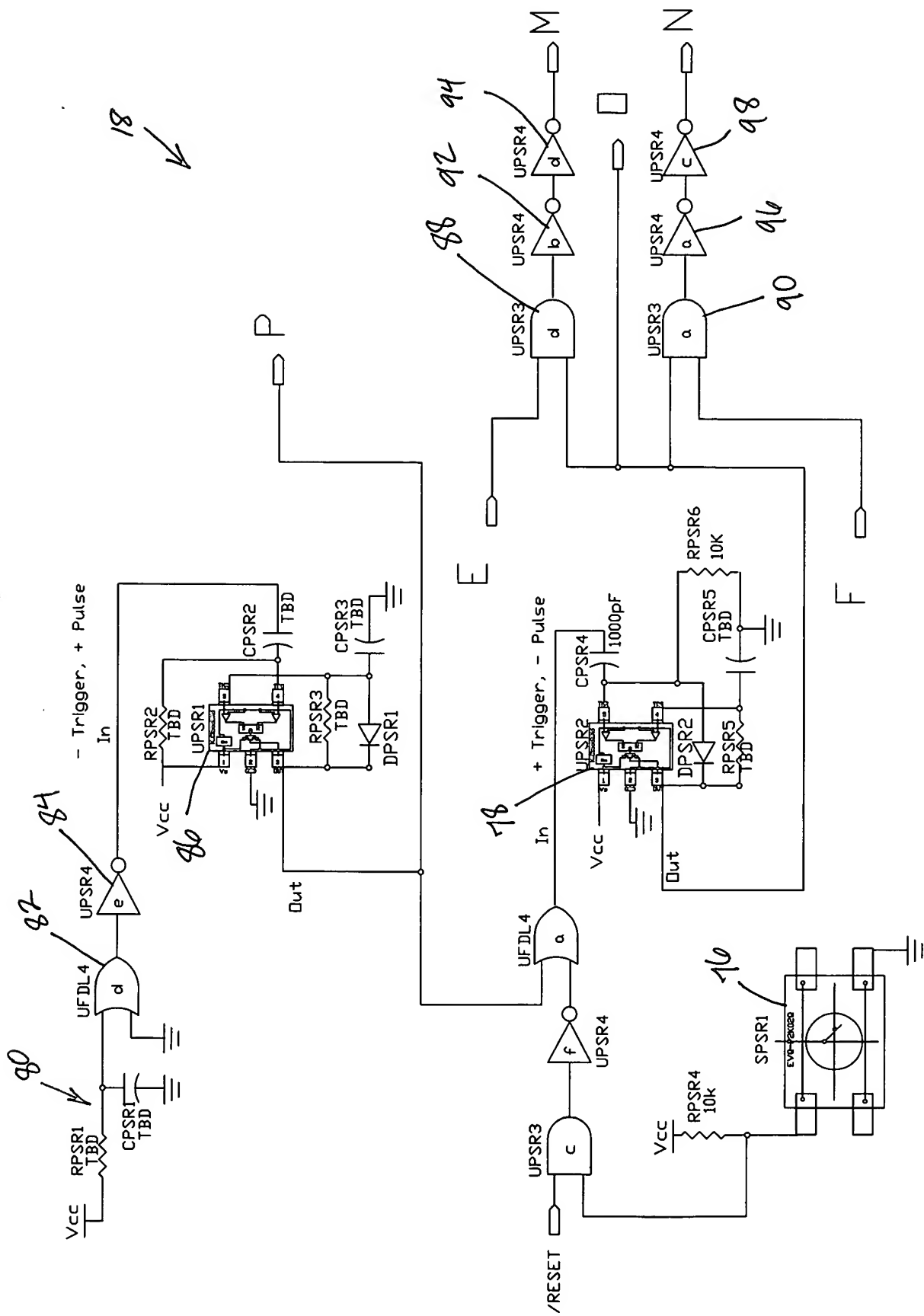


Figure 6 Power, Startup, Reset Stage

